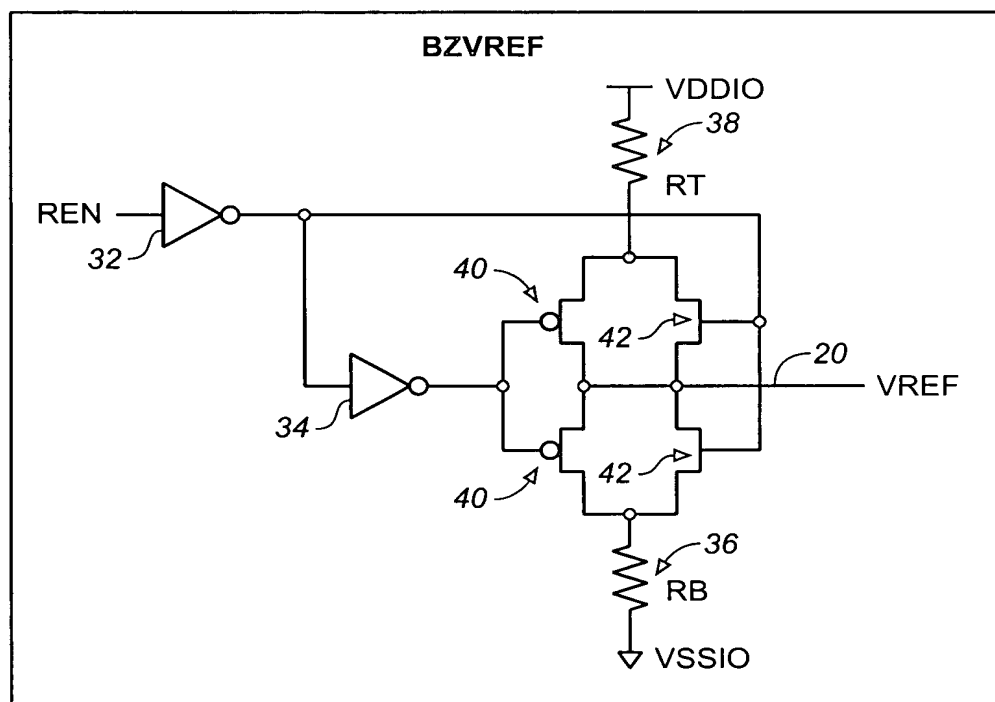


10 ↗

FIG._1

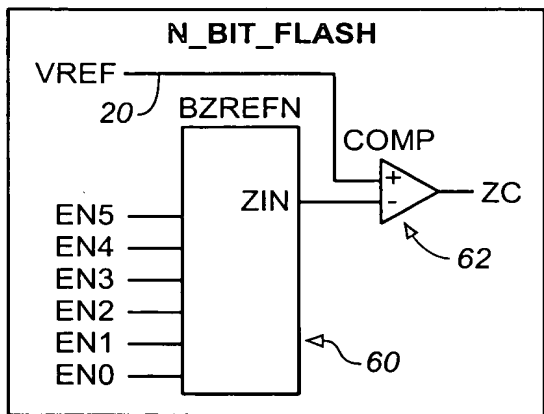


30 ↗

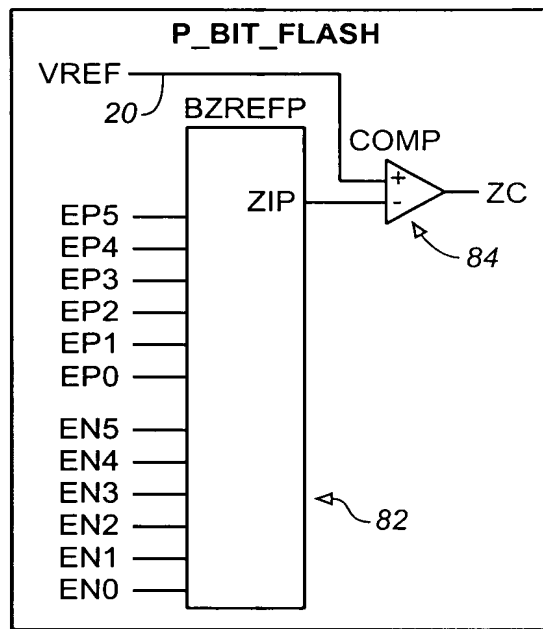
FIG._2



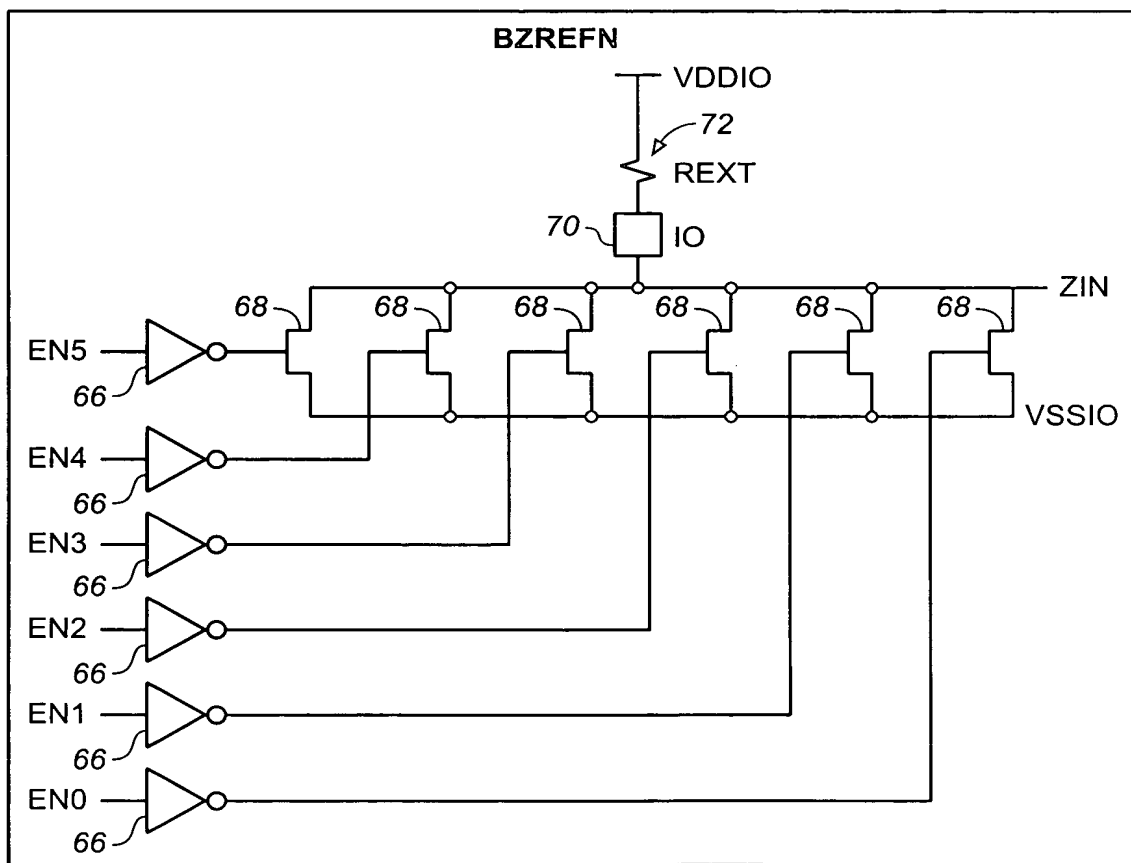
FIG. 3



50 → FIG._4



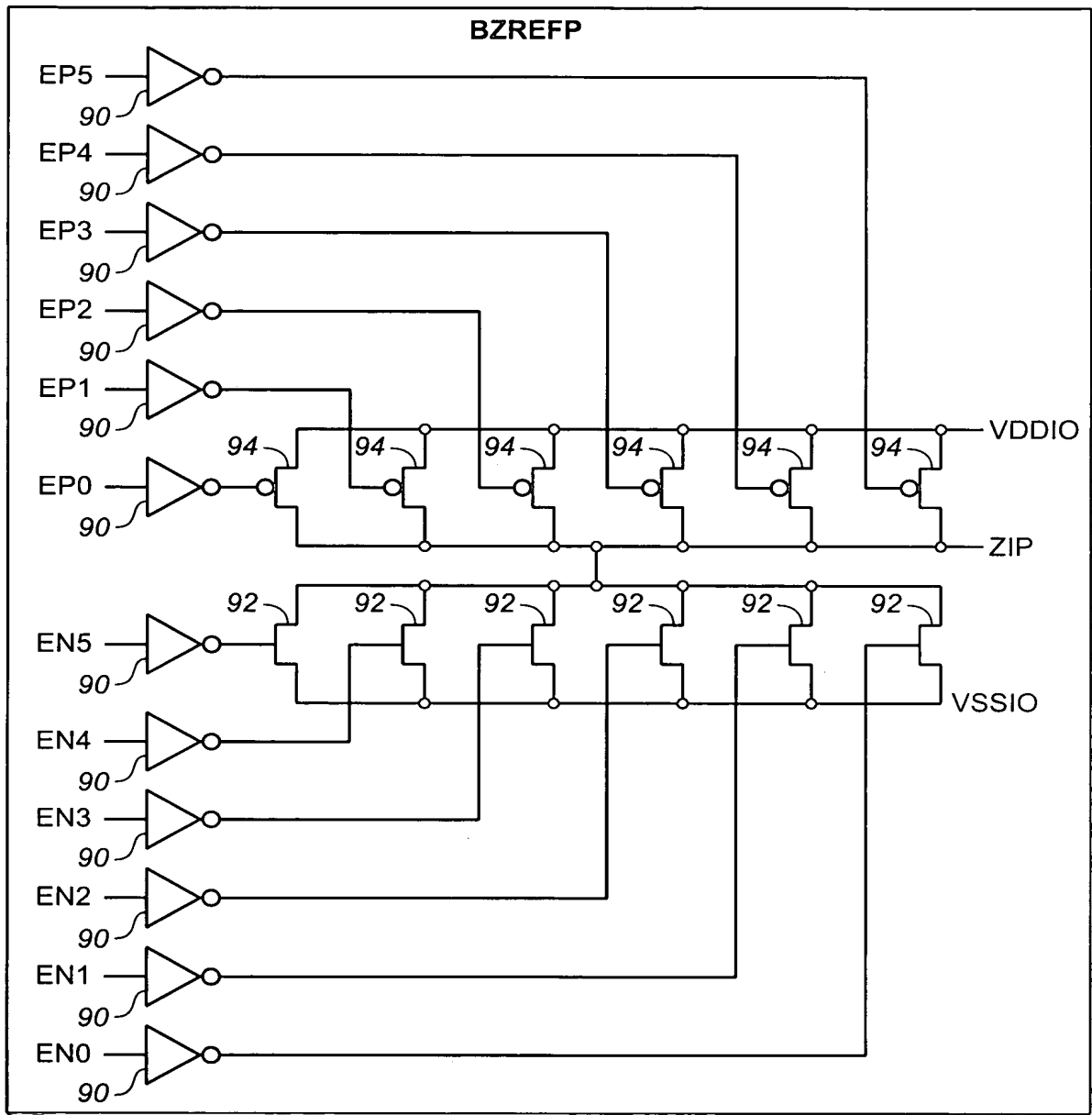
80 → FIG._7



60 → FIG._5



FIG. 6



82 ↗

FIG. 8



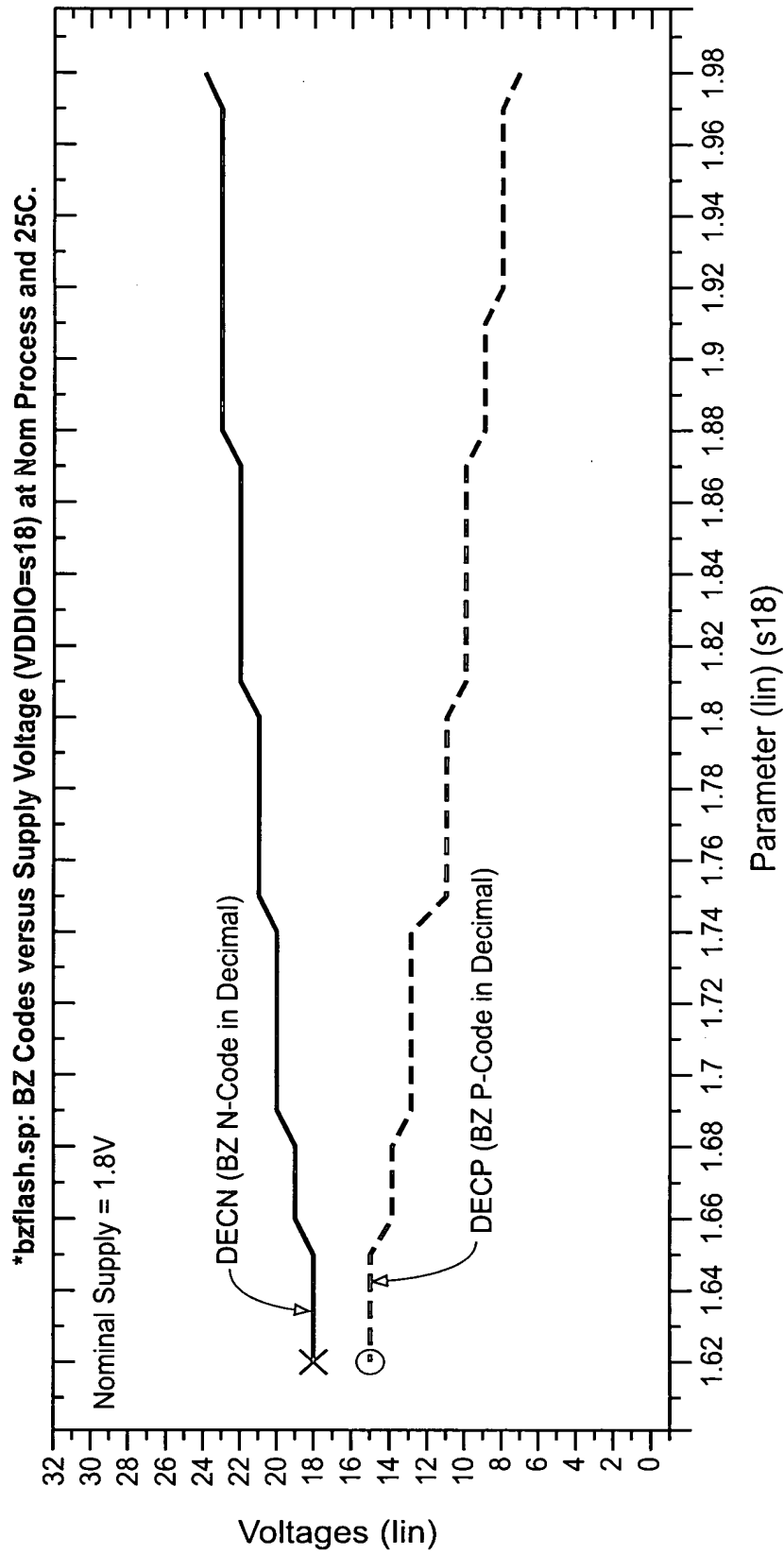


FIG. 9A

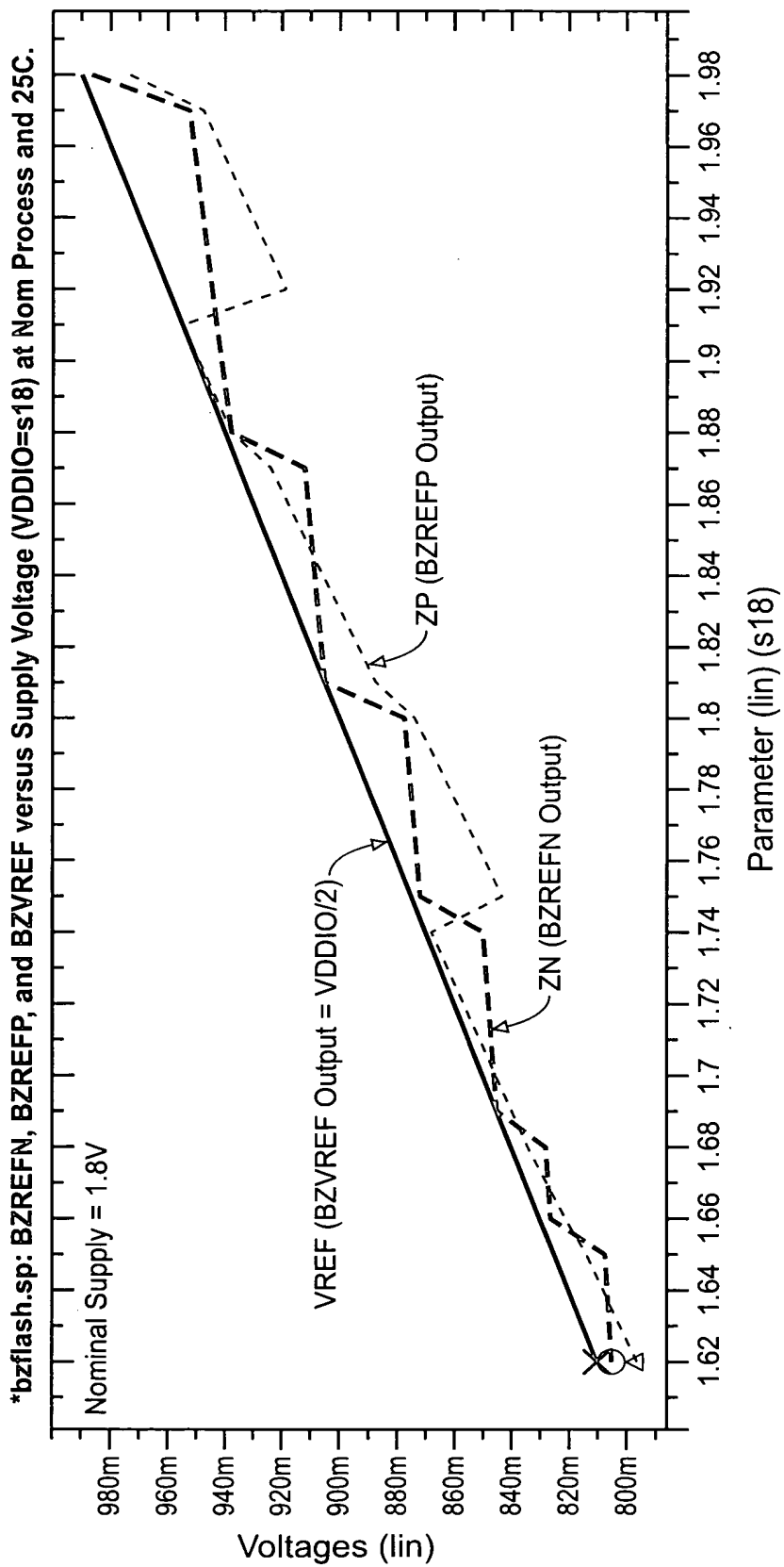


FIG. 9B

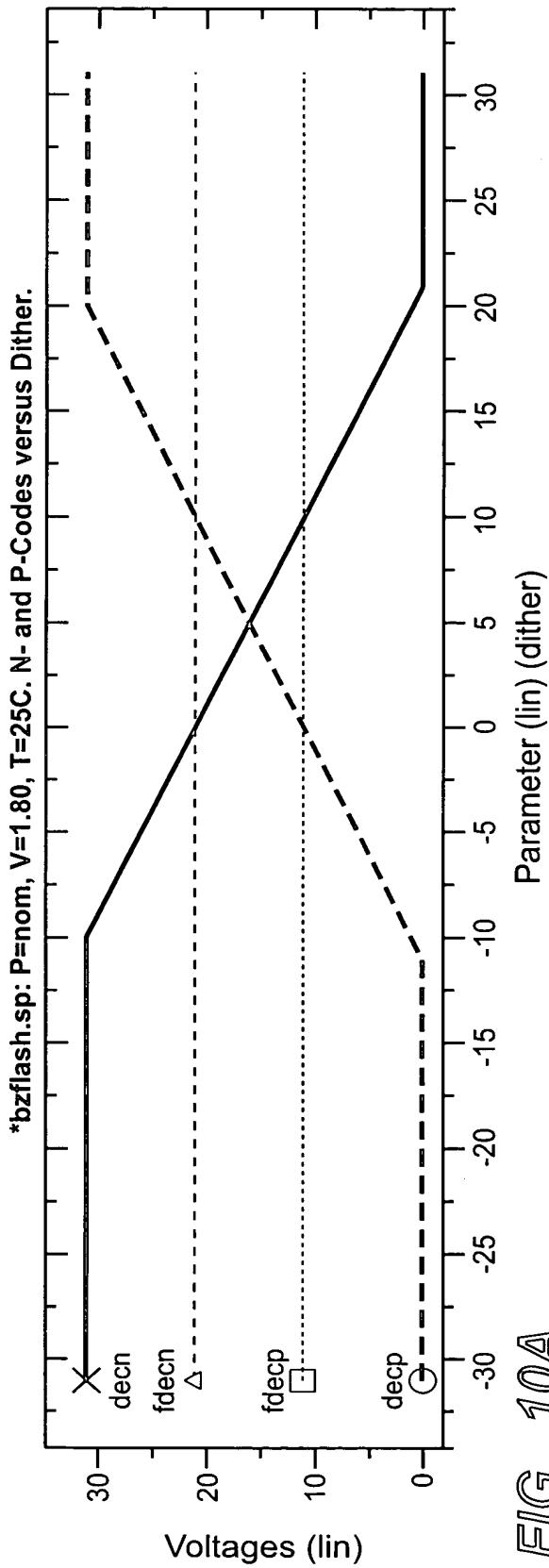
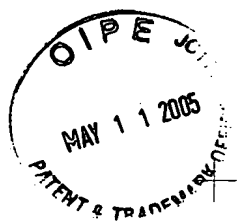


FIG. 10A

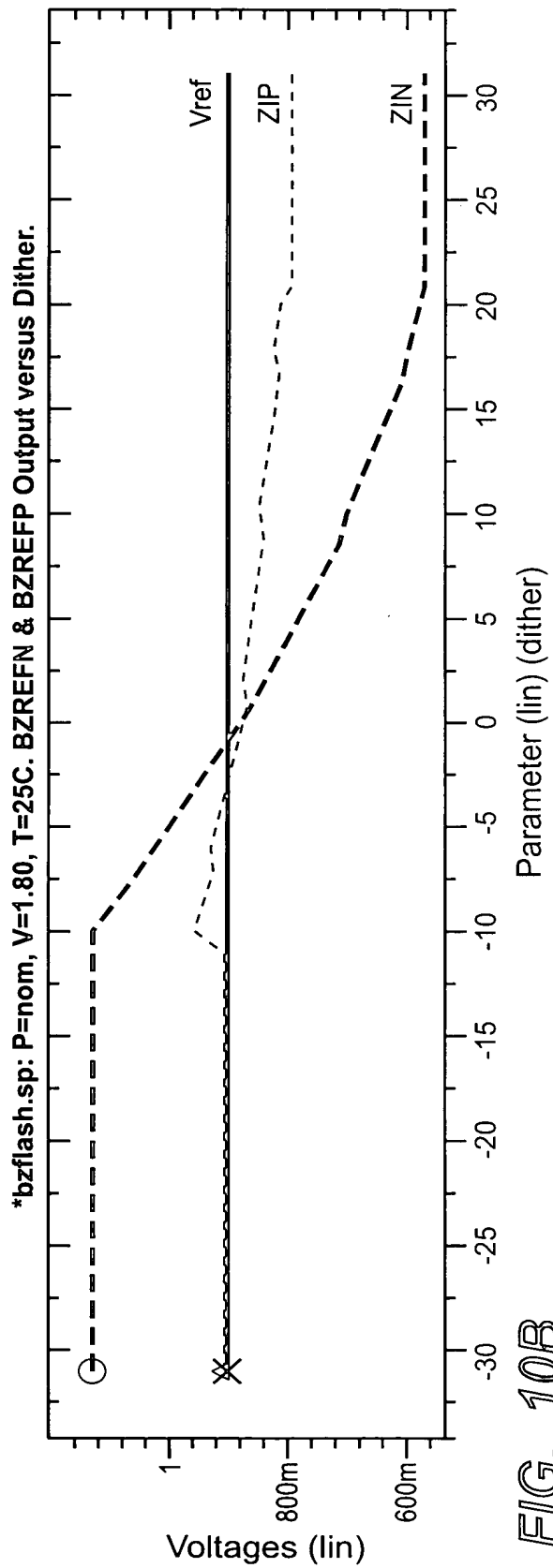


FIG. 10B

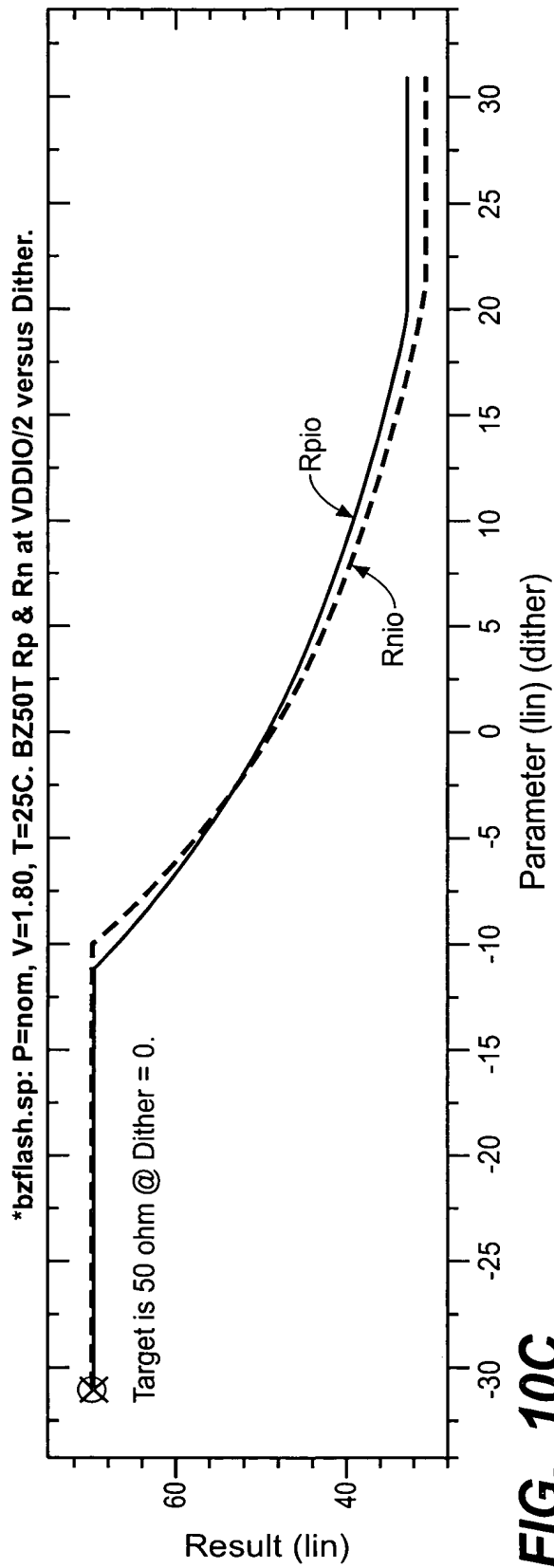


FIG._10C

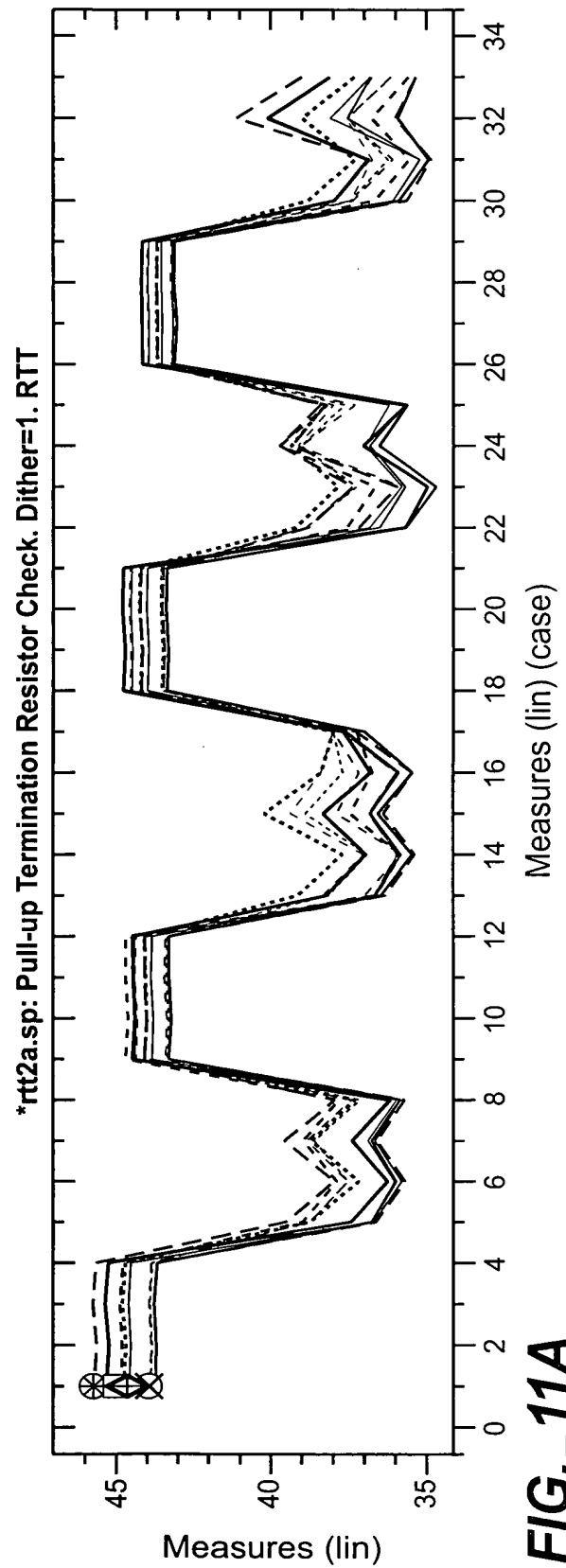


FIG._11A



*rtt2a.sp: Pull-up Termination Resistor Check. Dither=1. DECP.

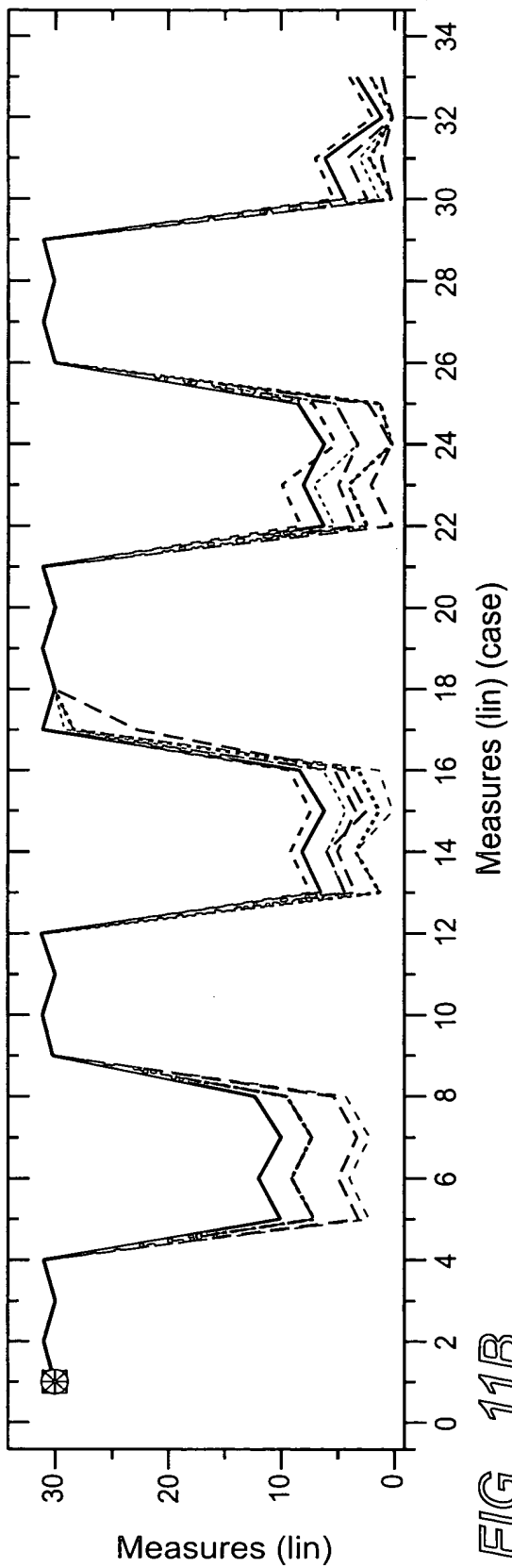


FIG. 11B

*rtt2a.sp: Pull-up Termination Resistor Check. Dither=1. DECN.

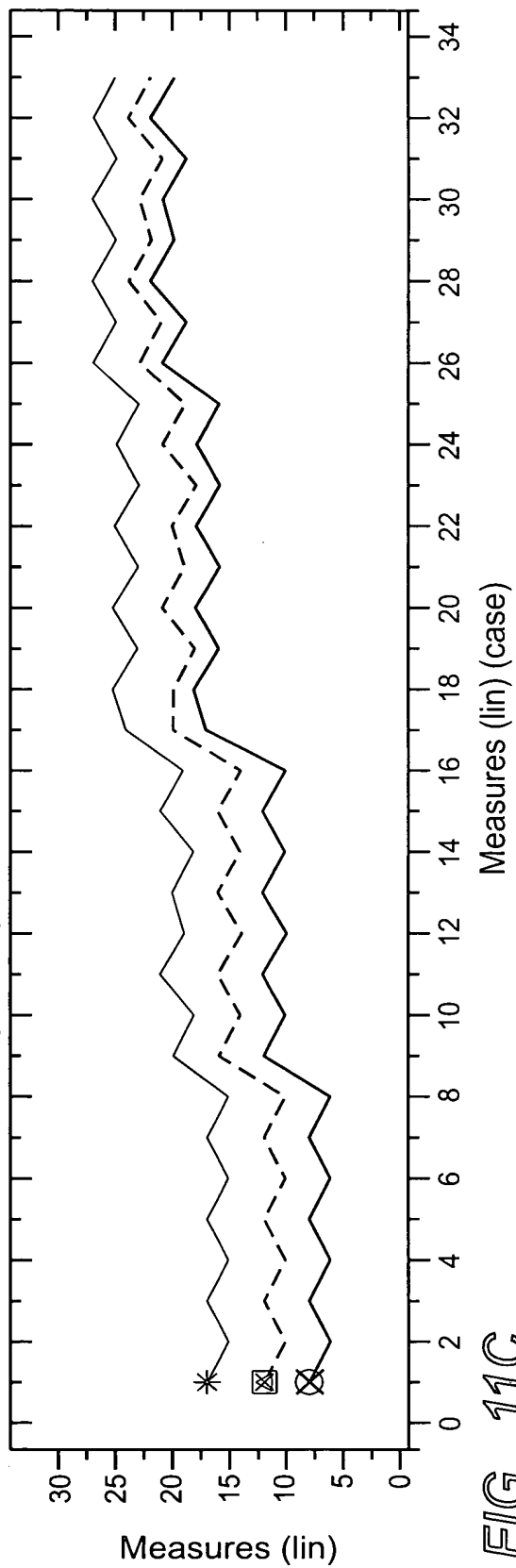
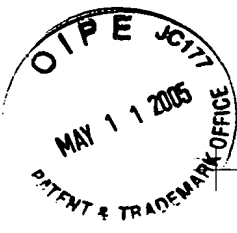


FIG. 11C



*rtt2a.sp: Pull-up Termination Resistor Check. Dither=1. TEMP.

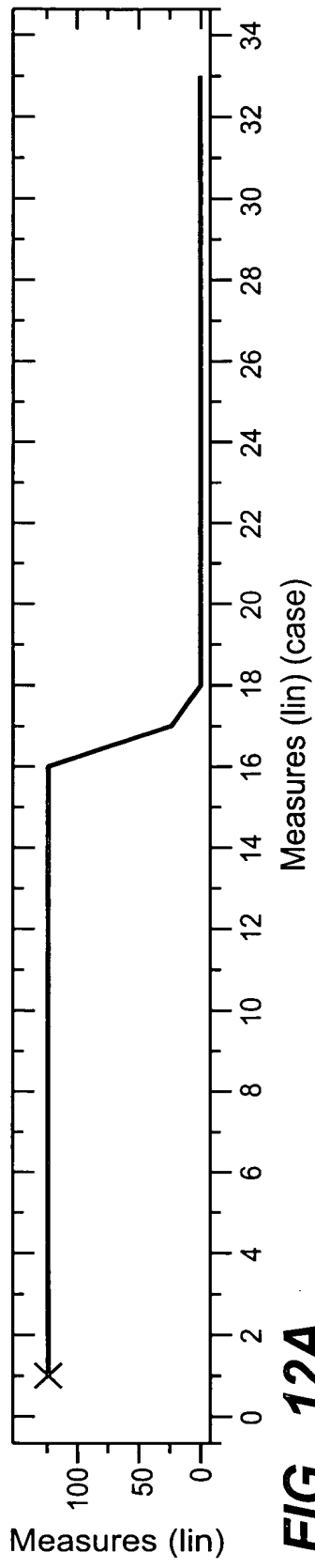


FIG. 12A

*rtt2a.sp: Pull-up Termination Resistor Check. Dither=1. VDD AND VDDIO.

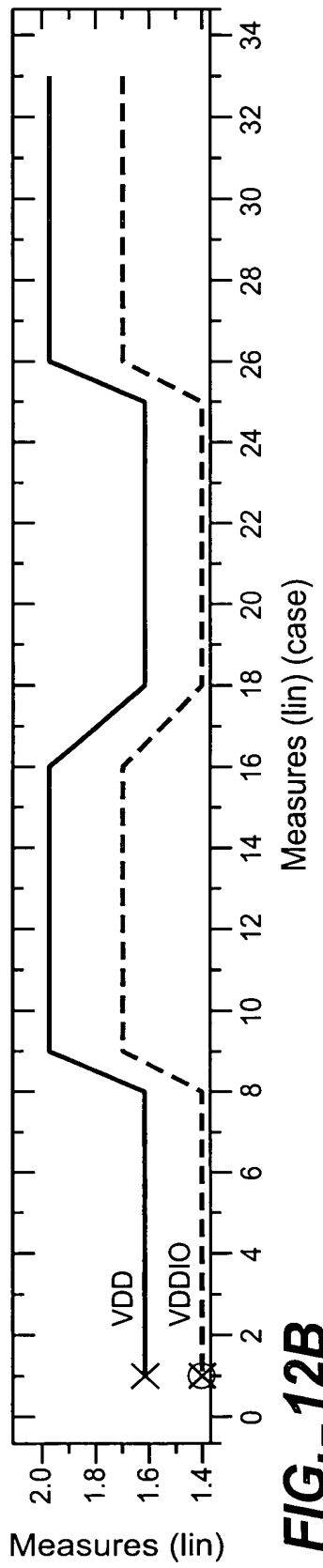


FIG. 12B

*rtt2a.sp: Pull-up Termination Resistor Check. Dither=1. RNPOLY (On-chip Resistor).

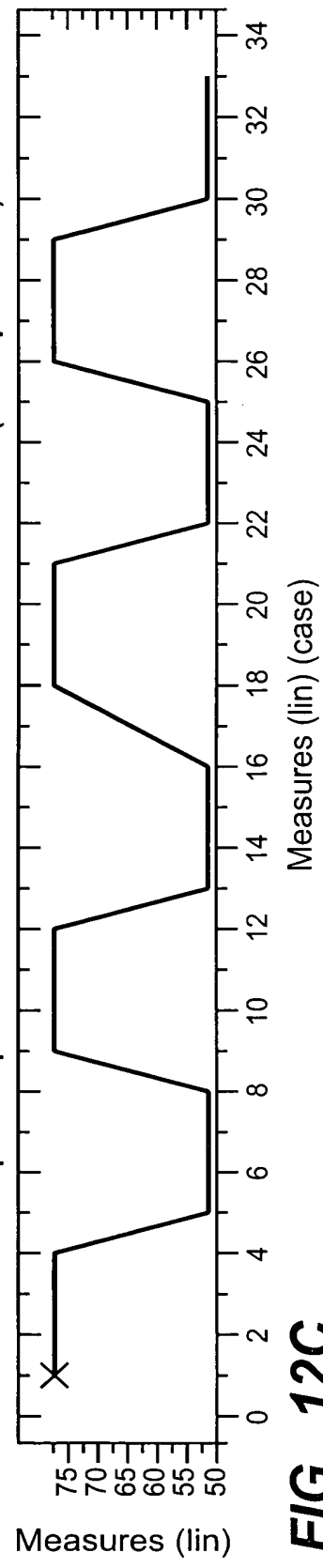


FIG. 12C



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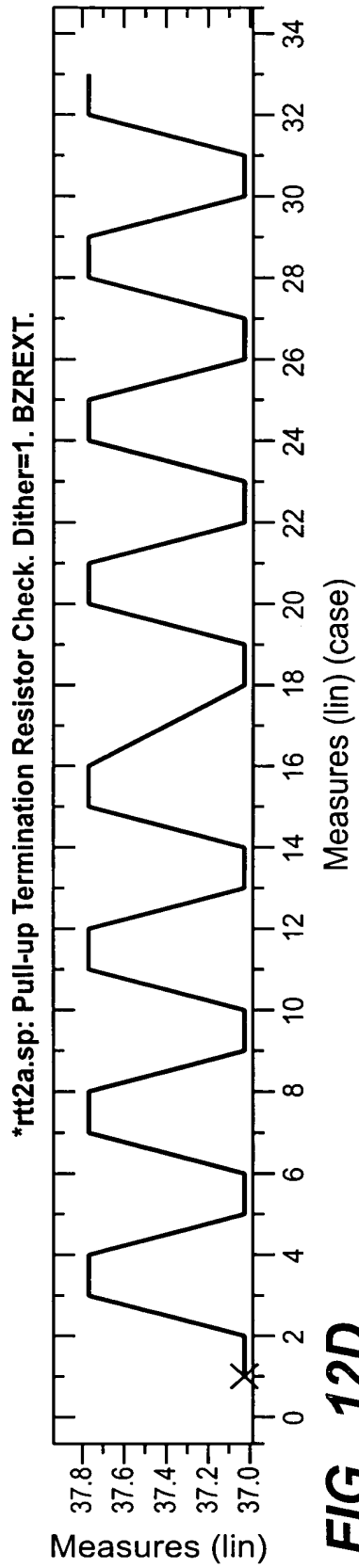


FIG._12D

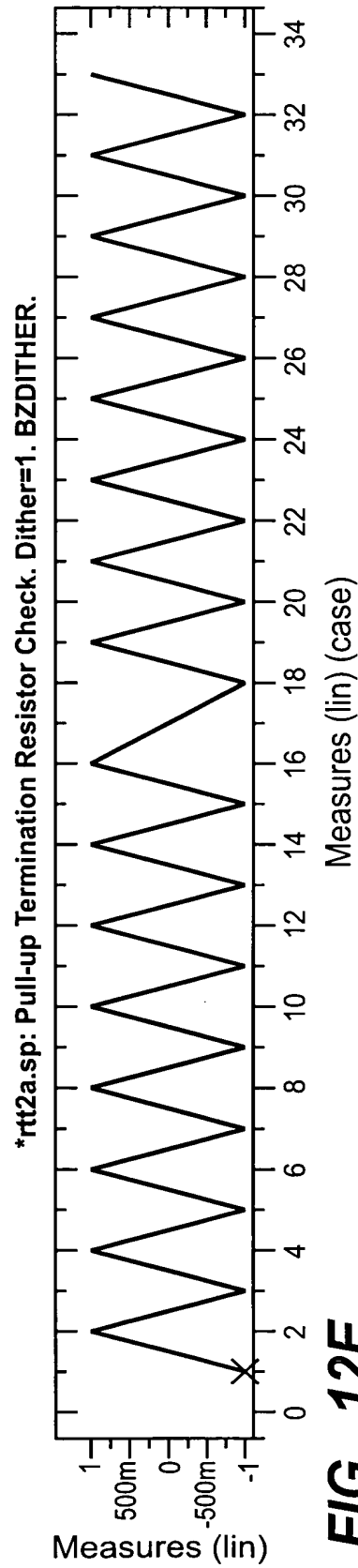


FIG._12E

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